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Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560

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JACOB, MARY C	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/620,045
Filing Date: July 15, 2003
Appellant(s): BHATTACHARYA ET AL.

MAILED

AUG 27 2007

Technology Center 2100

Joseph B. Ryan
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/21/07 appealing from the Office action mailed 11/17/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Boggio et al., "NetworkDesigner- Artifex- OptSim: A Suite of Integrated Software Tools for Synthesis and Analysis of High Speed Networks", Optical Networks Magazine, Sept/Oct 2001, pages 27-41

Sun et al., "Simulation Studies of Multiplexing and Demultiplexing Performance in ATM Switch Fabrics", Performance Engineering in Telecommunications Newtork Teletraffic Symposium, 14-16 April 1993, pages 21/1-21/5

Ishida et al., "A 10-GHz 8-b Multiplexer/Demultiplexer Chip Set for the SONET STS-192 System", IEEE Journal of Solid-State Circuits, Vol. 26, No. 12, Dec 1991, pages 1936-1943

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 3, 4, 6-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boggio et al in view of Sun et al.

As to Claims 1, 16, 18 and 19, Boggio et al teaches: a method of simulating the operation of an optical network and corresponding switching scheme (page 29, section 2, paragraph 4; page 30, column 1, paragraph 1, lines 11-15) comprising a plurality of integrated circuits (page 28, column 2, bullet 3; page 29, column 1, paragraph 5, sentence 3; page 30, column 2, lines 6-9), utilizing a software-based development tool, the method comprising the steps of: providing in the software-based development tool an interface permitting user control of one or more configurable parameters of the optical network (page 28, column 2, 4th and 5th bullets; page 29, section 2, paragraph 3); automatically generating a simulation configuration for the optical network based on current values of the configurable parameters, the simulation configuration being generated without requiring further user input, the simulation configuration specifying interconnections between the integrated circuits which satisfy the current values of the configurable parameters (page 30, column 1, lines 7-15). As to the storage, memory and processing device, since Boggio et al is directed to software tools running simulations including a debugger, report generator (page 30, column 1, lines 44-46), libraries (Figure 1, "Equipment Library") and displaying output on a graphical user

interface (Figure 12), it is understood that the software development tool must run on a computer system containing memory, processing device and a storage device.

As to Claim 6, Boggio et al teaches: wherein the interface includes a listing of the integrated circuits and permits user control of one or more configurable parameters of each of the integrated circuits (page 29, column 1, paragraph 5, sentence 3; page 30, column 1, lines 1-7).

As to Claim 7, Boggio et al teaches: wherein the interface includes a listing of a base device specified for the plurality of integrated circuits and permits user control of one or more configurable parameters of the base device (page 30, column 1, lines 1-7; page 10, column 2, lines 6-9).

As to Claim 12, Boggio et al teaches: wherein the software-based development tool comprises an automatic configuration generation module which generates the simulation configuration for the optical network based on the current values of the configurable parameters (page 30, column 1, lines 7-15).

As to Claim 13, Boggio et al teaches: wherein the simulation configuration is generated utilizing an object-oriented programming construct comprising a base class, corresponding to a base device specified for the plurality of integrated circuits, and an associated generation interface (page 30, column 1, lines 37-40; page 32, column 2, lines 27-35).

As to Claim 14, Boggio et al teaches: wherein the generation interface declares a generate function that is implemented by each of a plurality of generators, each of the

plurality of generators corresponding to a different configuration of the optical network (page 30, column 1, lines 7-15).

As to Claim 17, Boggio et al teaches: wherein the software-based development tool comprises a simulator control module (page 30, column 2, lines 3-5, 14-15), a set of interfaces (Figure 3; Figure 5; Figure 11), and circuit element modules each corresponding to an associated one of the integrated circuits (column 30, lines 6-9).

Boggio et al does not expressly teach (claims 1, 18, 19) simulating the operation of at least one switch fabric; (claim 3) wherein the at least one switch fabric comprises at least one multistage switch fabric; (claim 4) wherein the circuit elements comprise at least two ingress devices, at least one cross-connect device and at least two egress devices; (claims 8, 9, 10, 11) wherein the configurable parameters comprise a number of ports of the electronic system, switching capacity, configuration type, such as one of a centralized configuration, stackable configuration or distributed configuration; (claim 12) automatically generating the simulation configuration for the switch fabric based on the current values of configurable parameters; (claim 14) the plurality of generators corresponding to a different configuration of the switch fabric; (claim 15) the configuration types consisting of centralized configuration, stackable configuration or distributed configurations of the switch fabric.

Sun et al teaches (claims 1, 18, 19) a method for modeling a switch fabric with basic components for simulation to study multiplexing and demultiplexing performance in a network, enabling the switch fabric to be modeled without losing generality (Abstract), (claim 3) wherein the at least one switch fabric comprises a multistage switch

fabric, (claim 4) the integrated circuit elements comprise at least two ingress devices, at least one cross-connect device and at least two egress devices (Figure 2 and description), (claim 11) wherein the configurable parameters comprise a number of ports of the electronic system (Abstract, sentence 2; page 21/1, paragraph 6, sentence 4 and 5; page 21/2, paragraph 3), (claim 8) and switching capacity (Abstract, sentence 2; Figure 2; page 21/2, 3rd paragraph) ,(claim 9) a configuration type, (claim 10) use of a centralized configuration for a multistage switch fabric of the electronic system, (claims 14, 15) the ability to build other configurations (Figure 2, page 21/3, paragraph 1) and (claim 12) generating a simulation configuration for the switch fabric based on the current values of configurable parameters (pages 21/2-21/3 "Modelling Switching Fabrics").

Sun et al and Boggio et al are analogous art since they are both directed to the modeling and simulation of a network.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the software development tool for an optical network as disclosed in Boggio et al to include the modeling of a multistage switch fabric wherein the at least one switch fabric comprises a multistage switch fabric, the integrated circuit elements comprise at least two ingress devices, at least one cross-connect device and at least two egress devices, wherein the configurable parameters comprise a number of ports of the electronic system, switching capacity, a configuration type, the use of a centralized configuration for a multistage switch fabric of the electronic system, the ability to build other configurations and generating a simulation configuration for the

switch fabric based on the current values of configurable parameters as taught in Sun et al since Sun et al teaches a method for modeling a switch fabric with basic components for simulation to study multiplexing and demultiplexing performance in a network, enabling the switch fabric to be modeled without losing generality (Abstract).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boggio et al in view of Sun et al as applied to claim 1 above, and further in view of Ishida et al.

As to Claim 5, Boggio et al in view of Sun et al teach a software development tool for the automatic generation of a simulation configuration of a switch fabric including the specification between integrated circuits that satisfy configurable parameters.

Boggio et al in view of Sun et al does not expressly teach wherein the integrated circuits comprise integrated circuits of a designated chip set utilizable in the electronic system.

Ishida et al teaches an ultra high speed 8-b multiplexer and demultiplexer chip set that has been developed for the synchronous optical network (SONET) as a key component of next-generation optical fiber communication systems that will require higher data bit rates for future increases in transmission capacity (page 1936, column 1).

Boggio et al in view of Sun et al and Ishida et al are analogous art since they are both directed to the design of a communication network.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the design of the at least one switch fabric including user

configurable parameters of integrated circuits as taught by Boggio et al to include a chip set as taught in Ishida et al since Ishida et al teaches a high speed multiplexer and demultiplexer chip set that is a key component of a next-generation optical fiber communications systems that will require higher data bit rates for future increases in transmission capacity (page 1936, column 1).

(10) Response to Argument

Claims 1, 3, 4, 6-8, 11-13, 16-19

Appellant argues that the combined teachings of Boggio et al and Sun et al fail to teach or suggest, "providing a user interface permitting user control of one or more configurable parameters of a switch fabric" (page 4). The Examiner respectfully disagrees. The Examiner would like to begin by stating Boggio et al is relied upon to teach, "providing a user interface permitting user control of one or more configurable parameters for a data network. Examiner pointed to page 28, column 2, 4th and 5th bullets and page 29, section 2, paragraph 3 in Boggio et al where it is discussed that the NetworkDesigner tool, assessable via a graphical user interface (GUI), assists the network designer in specifying which parameters for the network design are fixed and variable, and also to describe or load information about the network layout, layers, resource location, users' location and traffic assumptions. The cited sections of Boggio et al also recite that the "scope of modeling", that is, the level of detail, can be "customized by the designer". Boggio et al teaches (section 2, paragraph 4) that with NetworkDesigner, protocols are chosen, switching schemes are specified and key

components are characterized. The Examiner asserts that these teachings of Boggio et al teach a "user interface permitting user control of one or more configurable parameters" for a data network. The teachings of Sun et al were relied upon to show a switch fabric that is modeled and simulated to study performance and to show that different configurations of a model for a switch fabric are possible as recited in the Grounds for Rejections above. The Examiner asserts that the combinations of the teachings of Boggio et al and Sun et al teach or suggest, "a user interface permitting user control of one or more configurable parameters of a switch fabric".

Appellant argues that the combined teachings of Boggio et al and Sun et al fail to teach or suggest "automatically generating a simulation configuration for the switch fabric specifying interconnections between the integrated circuits of the switch fabric" (page 4). The Examiner respectfully disagrees. The Examiner would like to begin by stating that Boggio et al was relied upon to teach "automatically generating a simulation configuration", the simulation configuration "specifying interconnections between integrated circuits" for a data network. As to the "automatic generation" of a "simulation configuration", Examiner points to Boggio et al, page 30, lines 7-15, wherein models of network components are "mapped" with OptSim or Artifex models for *immediate and automatic* execution of network level simulation, wherein the analysis is performed for the "network so far defined". The Examiner would like to point to Boggio et al, page 32, column 2, lines 17-26 for further insight as to this "automatic generation" of a "simulation configuration" and used by the Examiner to interpret the "mapping" of network

components with an Artifex model. The passage further describes this automatic generation of an Artifex model by the NetworkDesign tool, wherein Figure 5 shows the components of the network connected together, wherein the connections are based upon the "setting" of "specific model parameters", among them, "number of fibers" and "link length". The Examiner asserts these teachings of Boggio et al show an "automatic generation" of a "simulation configuration". As to "specifying interconnections between integrated circuits", the Examiner interprets "network so far defined" to be the network made up of both the "network components" and the routing, or "connections" between the network elements, that is specified by parameters set through the GUI of the NetworkDesign tool (as described in section 2, paragraphs 3 and 4) and by a chosen optimization technique (for example, such as shortest path for routing, section 2, paragraph 6). The Examiner also interprets "network components" or "network elements" to be integrated circuits wherein Boggio et al describes that the network components are available to the designer in device libraries (page 28, column 2, bullet 3) and teaches the network elements being mapped to OptSim components that include devices such as optical, electro-optical, electrical and logical components, including "signal processing elements" (page 30, column 2, lines 4-9). These components in the libraries are interpreted by the Examiner to be "integrated circuits". The Examiner asserts these teachings of Boggio et al teach specifying "interconnections between the integrated circuits" for a data network. The teachings of Sun et al were relied upon to show a switch fabric that is modeled and simulated to study performance and to show that different configurations of a model for a switch fabric are possible as recited in the

Grounds for Rejections above. The Examiner asserts that the combinations of the teachings of Boggio et al and Sun et al teach or suggest, "automatically generating a simulation configuration for a switch fabric specifying interconnections between the integrated circuits of a switch fabric"..

Appellant argues that the combined teachings of Boggio et al and Sun et al actively teach away from the limitations of "providing a user interface permitting user control of one or more configurable parameters of a switch fabric" and "generating a simulation configuration for the switch fabric specifying interconnections between the integrated circuits of the switch fabric" by disclosing arrangements with assume a single fixed switch fabric configuration (page 4). The Examiner would like to begin by noting that there is no limitation in the claims that require the generating of various different configurations for a switch fabric or for simulating more than one switch fabric. The claims are directed to a method of simulating the operation of "at least one switch fabric" and further recite the generation of "a" simulation configuration for "the switch fabric". The Examiner asserts that simulating the operation of a single switch fabric and generating a single simulation configuration is all that is required to be shown by the prior art in order to meet the limitations of the claims. Further, the Examiner asserts that the combined teachings of Boggio et al and Sun et al do not teach away from these limitations. The teachings of Boggio et al, which is relied upon to show the automatic generation of a simulation configuration, does not describe the simulation of a fixed configuration, it teaches different configurations of a network being simulated based on

the parameters specified by the user (section 2, paragraph 3, "Network layout...can be manually described...", page 32, column 2, lines 17-26). Appellant recites passages of Boggio et al that teaches "network elements" that are modeled having a "fixed back-plane", however, this is referring to how the "network elements" themselves are modeled, not that the interconnections between the network elements are fixed. The Examiner agrees that Sun et al teaches the modeling of a single switch fabric configuration (Figure 2) using a fixed routing mechanism (page 21/3, paragraph 6), yet, Sun et al further recites that "other configurations" and "more complicated" models of a switch fabric can be built (page 21/3, first paragraph) and that more complicated routing mechanisms can be used, showing that it is known in the art to simulate various configurations of switch fabrics with other routing mechanisms.

Prima Facie Case Established

Before discussing Appellant's additional arguments (pages 5 and 6), the Examiner would like to establish the thought process that was used in establishing a prima facie case for this particular application. Referring to the first Office Action on the merits, dated 6/19/06, Examiner relied upon the teachings of Boggio et al to show, "a method of simulating the operation of an *electronic system* comprising a plurality of *circuit elements*", "an interface permitting user control of one or more configurable parameters of the *electronic system*", "automatically generating a simulation configuration for the *electronic system* based on current values of the configurable parameters", "the simulation configuration being generated without requiring further user

input" and "the simulation configuration specifying interconnections between *the circuit elements* which satisfy the current values of the configurable parameters" in a rejection under 35 U.S.C. 102(b). Appellant responded on 9/19/06 by amending the claims to change "electronic system" to "switch fabric" and "circuit elements" to "integrated circuits". Examiner would also like to point out that the Appellant's 9/19/06 remarks recite Boggio et al "appears to represent non-analogous art relative to the claimed invention" and that Sun et al "teaches away from the added limitations by teaching the use of a single switch fabric configuration". Appellant did not recite arguments as to why Boggio et al does not teach the limitations of "a method of simulating the operation of an *electronic system* comprising a plurality of *circuit elements*", "an interface permitting user control of one or more configurable parameters of the *electronic system*", "automatically generating a simulation configuration for the *electronic system* based on current values of the configurable parameters", "the simulation configuration being generated without requiring further user input" and "the simulation configuration specifying interconnections between *the circuit elements* which satisfy the current values of the configurable parameters". Therefore, in the Final Rejection dated 11/17/06, the Examiner changed the rejection of the independent claims 1, 18 and 19 under 35 U.S.C. 102(b) in view of Boggio et al to a rejection under 35 U.S.C. 103 as anticipated by Boggio et al in view of Sun et al wherein Sun et al teaches the simulation of a switch fabric. The Examiner responded in the Final Office action dated 11/17/06 by pointing out that Appellant's arguments do not clearly point out the patentable novelty of the claimed invention in view of the state of the art disclosed by the referenced cited

and responded to the arguments regarding the Sun et al reference. Examiner asserts that a proper prima facie case was established as further discussed below.

Appellants responded after the Final Office action by filing remarks on 2/20/07 reciting arguments that the Examiner determined to be non-persuasive, and responded to in an Advisory Action, dated 3/14/07. These arguments are now being further addressed in this Examiner's Answer.

Appellant argues Sun et al and Boggio et al are not analogous prior art and therefore cannot form the basis for a rejection under 35 U.S.C. 103 (page 5). The Examiner asserts that the art are considered analogous since they are both in the same field of endeavor, that is, the modeling and simulation a system such as a data network. Further, the Examiner asserts that since these arts are considered analogous, a reasonable expectation of success would be present in the combinations of the teachings.

Appellant argues that Boggio et al and Sun et al do not disclose the limitations of claim 1 (page 5). It is the Examiner's position that all limitations have been addressed and are supported by the prior art of record.

Appellant argues that the Examiner does not provide sufficient objective motivation for the combination and that impermissible hindsight was used by the Examiner to combine the teachings of the prior art (page 6). The Examiner directed Appellant to Sun et al who states that their method of modeling a switch fabric for simulation is used to study the multiplexing and demultiplexing performance in a

network (Abstract). It is the Examiner's position that this statement provides adequate suggestion or motivation to combine the teachings of Boggio et al and the teachings of Sun et al since it would be obvious to simulate a data network such as a switch fabric with the method of simulating a data network as taught in Boggio et al since both arts are directed to studying the performance of a data network using simulation techniques.

The Examiner contends that a prima facie case of obviousness has been established and the rejection is proper.

Claim 9

Appellant argues that the combined teachings of Boggio et al and Sun et al fail to teach or suggest providing an interface permitting user control of a configuration type of the switch fabric and automatically generating a simulation configuration for the switch fabric based on a current value for the configuration type. To this point, Appellant argues, "Sun fails to disclose an interface permitting user control of a configuration type, much less automatically generating a simulation configuration based on a current value of the configuration type" (page8). The Examiner asserts that Boggio et al (section 2, paragraph 3) is relied upon to show an interface that permits user control of configurable parameters, wherein the configurable parameters may include a "network layout", wherein the "network layout" is considered a "configuration" of the network. Further, the teachings of Sun et al (page 21/3, paragraph 1) teach that "different configurations" of the switch fabric to be modeled and simulated are possible. Therefore, it is known in the art to simulate different configurations of a switch fabric.

The Examiner contends that the combined teachings of Boggio et al and Sun et al teach or suggest this limitation.

Claim 10

Appellant argues that the combined teachings of Boggio et al and Sun et al fail to teach or suggest the interface permitting user selection of one of a centralized configuration, a stackable configuration and a distributed configuration for a switch fabric. To this point, Appellant argues, "Sun fails to disclose an interface permitting user selection of a configuration type, much less of a centralized configuration, a stackable configuration and a distributed configuration for the switch fabric" (page 8). The Examiner would first like to point out that the claim language only requires user selection of "one of" the configurations, not all three. The Examiner asserts that Boggio et al (section 2, paragraph 3) is relied upon to show an interface that permits user control of configurable parameters, wherein the configurable parameters may include a "network layout", wherein the "network layout" is considered a "configuration" of the network. Further, the teachings of Sun et al (page 21/3, paragraph 1) teach that "different configurations" of the switch fabric to be modeled and simulated are possible. As to the centralized, stackable and distributed configuration, the Examiner looked to the specification for further clarification. In reading page 9, lines 3-20 and considering Figure 5, the Examiner interpreted a "centralized configuration" to be a configuration in which one or more "cross-connect" devices route traffic between the ingress devices and the egress devices. Based on this interpretation, Examiner concluded that Sun et

al, Figure 2, discloses a "centralized configuration" for a switch fabric. Therefore, the examiner asserts that the combined teachings of Boggio et al and Sun et al teach or suggest a user interface permitting user selection of one of a centralized configuration, a stackable configuration and a distributed configuration for a switch fabric.

Claim 14

Appellant argues that the combined teachings of Boggio et al and Sun et al fail to teach or suggest wherein a generation interface declares a generate function that is implemented by each of a plurality of generators, each of the plurality of generators corresponding to a different configuration of the switch fabric. To this point, Appellant further argues that Sun does not teach or suggest the implementation of the plurality of generators (page 9). The Examiner contends that the combined teachings of Boggio et al and Sun et al suggest or teach this limitation. The teachings of Boggio et al recite that "network layout" is defined by the user (section 2, paragraph 3), therefore, this specification of a "network configuration" implements a "generate function" to in the NetworkDesign tool to generate the network layout defined by the user. Further, the teachings of Sun et al (page 21/3, paragraph 1) discuss that other configurations of a switch fabric are possible for modeling and simulation. The Examiner asserts that although Sun et al does not expressly teach a "plurality of generators", it would be obvious to one of ordinary skill in the art to generate different configurations of a switch fabric for modeling and simulation.

Claim 15

Appellant argues that the combined teachings of Boggio et al and Sun et al fail to teach or suggest wherein the interface permits user selection of a configuration for the switch fabric (page 10). The Examiner notes that the "user selection" is not recited in the claim language of claim 15, nor is it recited in claims 1, 13 or 14. Examiner discusses this argument in response to the arguments for claim 10 above. Appellant further argues that Sun et al does not teach an implementation wherein a plurality of generators comprises a centralized, stackable and distributed generator corresponding to the respective configurations of the switch fabric (page 10). The Examiner discussed the arguments regarding the plurality of generators in response to the arguments for claim 14 above. With regard to the different configurations, the teachings of Sun et al (page 21/3, paragraph 1) discuss that other configurations of a switch fabric are possible for modeling and simulation. The Examiner asserts that although Sun et al does not expressly teach a plurality of generators, it would be obvious to one of ordinary skill in the art to generate different configurations of a switch fabric for modeling and simulation, including centralized, distributed and stackable configurations.

Claim 5

Appellant argues that Ishida et al fails to teach or suggest the additional limitation of wherein the integrated circuits comprise integrated circuits of a designated chip set utilizable in the switch fabric. Examiner asserts that the combined teachings of Boggio et al in view of Sun et al in further view of.Ishida et al teach or suggest this limitation.

Boggio et al in view of Sun et al teach the automatic generation of simulation configurations for a data network wherein the simulation configuration specifies interconnections between the integrated circuits in the data network. Ishida et al teaches a data network comprising a designated chip set. The Examiner contends that it would have been obvious to one of ordinary skill in the art to modify the simulations of the data network as taught in Boggio et al in view of Sun et al to include integrated circuits from a designated chip set as taught in Ishida et al.

Further Considerations

Although not relied upon for the rejections of the claims, the Examiner would like to submit additional references that are considered pertinent to Appellant's disclosure:

Krishnamurthy et al ("Dynamic Reconfiguration of an Optical Interconnect", Proceedings of the 36th Annual Simulation Symposium", March 300-April 2, 3003) teaches a simulation based performance of a switch fabric constructed using optical technology for communicating between CMOS chips that implement the fabric (Introduction, paragraph 4, section 2, paragraphs 1 and 3). Krishnamurthy et al teaches the ability to reconfigure the switch fabric (Introduction, paragraph 5), and the modeling and simulation of the switch fabric including reconfiguring the system with a "reconfiguration parameter" (section 3.2, paragraph 2, sentences 1-3). The Examiner contends that this reference shows that switch fabrics are used in optical networks and further, teaches a configurable parameter, set by a user that will generate a simulation configuration for a switch fabric.

Ye et al ("Analysis of Power Consumption on Switch Fabrics in Network Routers", DAC 2002, June 10-14 2002, New Orleans, LA) teaches the modeling and simulation of four different switch fabric architectures using Simulink (Abstract, section 5.2, paragraphs 2 and 5).

For the above reasons, it is believed that the rejections should be sustained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Respectfully submitted,

Mary C. Jacob

Mary C. Jacob

Examiner, Art Unit 2123

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

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Conferees:

Paul L. Rodriguez

SPE, Art Unit 2123

Eddie Lee

Appeals Specialist, TC2100

EDDIE C. LEE
SUPERVISORY PATENT EXAMINER

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